PROJECT PROFILE



2T305: Full assessment of nanoimprint technology addressing sub-35 nm ICs (FANTASTIC)

LITHOGRAPHY

Partners:

AMO AMTC ASML CEA-LETI **DNP** Photomask Europe EV Group Fraunhofer CNT Fraunhofer Institute IMEC IMS CHIPS Infineon Technologies LTM-UIF Microresist Technology Molecular Imprints Nawotec NXP Semiconductors Qimonda **STMicroelectronics** Vistec Electron Beam Vistec Semiconductor

Project leader:

Serge Tedesco CEA-LETI

Key project dates:

Start: July 2006 End: February 2009

Countries involved:

Austria Belgium France Germany Italy The Netherlands Despite recent advances in immersion technologies for chipmaking, conventional optical lithographic processes are reaching their physical limits. Emerging ultraviolet nanoimprint technology now offers a potentially different and cheaper approach to next generation lithography for high resolution micro- and nanoelectronics applications. The MEDEA+ FANTASTIC project will evaluate all aspects of this new technique – both technical and economic – for CMOS applications at the 32 nm half pitch technology level and beyond. Success could open up an alternative to extreme ultraviolet (EUV) lithography for future wafer-patterning processes – and provide support for equipment and materials suppliers.

The global microelectronics industry's demand for systems based on ever greater integration in ever smaller devices has not diminished over the years. However manufacturing increasingly small devices requires cost-effective processing techniques. Several alternative technologies have been proposed for next generation lithography but the costs involved in developing equipment that includes tools, optics and materials are horrendous.

Ultraviolet (UV) nanoimprint techniques appear to offer one economic alternative. This approach uses mechanical embossing methods to print circuit patterns with resolutions beyond the limitations caused by light diffraction or beam scattering in conventional optical lithography. After imprinting, the patterned polymer resist is cured by UV light projected through the quartz mask or template, hardening into the device patterns required for etching. Patterns are written on the template using an electron beam with the same line width as that of the pattern on the wafer rather than reducing it by four times as with conventional optical lithography.

Nanoimprinting enables patterning of features below 32nm half pitch. Moreover, these techniques offer a three-dimensional (3D) printing capability that could be exploited by:

- Replacing several complex time- and cost-consuming fabrication steps by a single nanoimprint operation, cutting overall cycle times and associated processing costs – and thus reducing total cost of ownership; and
- Printing specific shapes on the wafer that are not feasible today and that could offer additional circuit functionalities.

In addition to offering advantages in terms of reduced tool complexity, the technological requirements of nanoimprinting in terms of process environmental conditions are markedly lower than with optical lithography. And, by avoiding expensive optics and cumbersome enhancement techniques such as phase-shift masks, the machines can cost far less than current step-and-scan systems.

Overcoming lack of information

The potential for UV nanoimprint technology is already acknowledged in the international technology roadmap for semiconductors (ITRS) as one of the potential next generation lithographic tools for 32 nm half pitch. Full production of 32 nm half pitch technology is forecast to commence in 2013 with process development starting by 2010. This means that process selection must be completed in 2008.

A key candidate is still extreme UV (EUV) lithography using 13.5 nm wavelength soft X-rays, but the costs are high. UV nanoimprint appears to offer a competitive alternative for production of small series products.

However, there is considerable hesitation about nanoimprint technology within the semiconductor industry itself. This results from the lack of significant information on tools and on template fabrication – for example, producing a defectfree quartz mask with a complex pattern of features at 50 nm and below poses considerable challenges. While isolated solutions exist, the interfaces in the process chain must be completed and an industrial level achieved. Suitable criticaldimension measurement, overlay control and defect inspection equipment also need to be developed.

The MEDEA+ 2T305 FANTASTIC project is therefore carrying out a detailed assessment of the UV nanoimprint process in terms of technological ability, required effort to provide manufacturing solutions and the potential cost of ownership. The project will investigate all aspects of the technology involved: the manufacturing tool, the imprint process, template fabrication – including patterning, inspection and repair – and, finally, process integration. The ultimate step will be demonstrations of the patterning of both a contact-hole layer and of a dual-damascene interconnect layer.

Driven by chipmakers

FANTASTIC involves the main production equipment suppliers, maskmaking shops and major microelectronics research institutes engaged in nanoimprint activities and will be driven by the leading European semiconductor manufacturers. If the project clearly demonstrates the potential of UV nanoimprint technology for CMOS applications at the sub-50 nm half pitch, a follow-up project is planned to establish the full infrastructure for volume production at 32 nm half pitch.

Many of the partners in FANTASTIC have been involved in earlier UV nanoimprint and high resolution patterning research. The MEDEA+ project will build on the know how, equipment and materials developed in such work, including the EU CRAFT 3D NanoPrint and Framework Programme NaPa emerging nanopatterning methods projects, and the German UVNIL and MINALI projects.

Work in FANTASTIC is split across four work packages covering:

- Tools: including both the optimisation of existing tools and the development of a new tool environment to enable the realisation of a CMOS application;
- Imprint process development: dealing with tools, resists and the process platform for UV nanoimprint lithography – including development of low-k resists for dual-damascene technology – as well as investigating the use of 3D templates;
- 3. Template fabrication: covering all

aspects including substrates, exposure, resists and etching processes, inspection, repair and cleaning; and

4. Integration: bringing together all the elements to enable the realisation of a contact-hole layer and a dual-damascene interconnect level within an existing 300 mm wafer size CMOS technology. The results in terms of yield, defects, alignment and parametric results will indicate the real benefits, limitations and areas for improvement in UV nanoimprint technology.

Advanced access to equipment

Early access to advanced lithography technology is vital for European competitiveness. New manufacturing technology for fast, low cost and reliable high volume production of nanoelectronics devices is essential to help promote sustainable industrial growth, significantly enhance Europe's economy and have a major impact on employment.

Selection of the right lithographic process is therefore crucial to enable the European semiconductor industry to maintain or even improve its global position in the next decade. This MEDEA+ project will provide the major European chipmakers with early access to a costeffective processing platform for 32 nm devices. Moreover, the results of FANTAS-TIC will encourage European equipment and materials supplier to develop all the necessary tools to prepare the infrastructure and basic know how essential to enable them to gain an increased share of the global market at this level.



MEDEA+ Office 140bis, Rue de Rennes F-75006 Paris France Tel.: +33 1 40 64 45 60 Fax: +33 1 40 64 45 89 Email: medeaplus@medeaplus.org http://www.medeaplus.org



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